USN | | | | | | | | | | |

10EC751

Seventh Semester B.E. Degree Examination, June/July 2017

DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the major architectural features of programmable Digital Signal Processing devices. **(08 Marks)**

b. With the help of block diagram explain the digital filter. **(04 Marks)**

c. An FIR filter is described by differential equation. $y(n) = 0.6\ x(n) + 0.6\ x(n-1)$. Determine system function, frequency response, impulse response, magnitude response function and phase response. **(08 Marks)**

2 a. Draw the structure of 4 × 4 Braun multiplier and explain its operation. **(08 Marks)**

b. Describe the implementation of single MAC unit for an 8-tap (coefficient) FIR filter. **(08 Marks)**

c. Find the total time required to compute the sum of 250 products using pipelined MAC unit. The MAC unit execution time is 100 nsec. **(04 Marks)**

3 a. What is meant by addressing mode? Explain absolute, accumulator and direct addressing modes of TMS 320C54×× processor. **(08 Marks)**

b. Describe the operations of the following :

i) MPY *AR2 - , * AR4 + O. B

ii) MAC * AR3 - , * AR4 +, B. A

iii) MAS * AR3 -, * AR4 + B, A **(06 Marks)**

c. Explain the hardware timer of TMS 320 C54×× DSP with logical block diagram. **(06 Marks)**

4 a. What are the different types of serial I/O ports in C54××? Explain the application of each serial I/O port. **(08 Marks)**

b. With a neat diagram, describe the different stages of pipelining in C54×× processors. **(08 Marks)**

c. Write a TMS 320C54 ×× ALP o find a sum of a set of 4 numbers stored in on array labeled 'num'. **(04 Marks)**

PART – B

5 a. What is the significance of Q-notation in DSP? **(04 Marks)**

b. Explain the IVth order FIR filter implementation with the organization of samples and filter coefficients in circular buffer. **(10 Marks)**

c. What is interpolation? Explain the interpolation process to implement interpolation filter with interpolation factor 'L'. **(06 Marks)**

6 a. Determine the following for 128 point FFT computation.
   i) Number of stages
   ii) Number of butterflies in each stags
   iii) Number of butterflies needed for the entire computation
   iv) Number of butterflies that need on multiplication. **(04 Marks)**

   b. Explain how the bit reversed index generation can be done in an 8-point DFT computation. **(06 Marks)**

   c. What is the need for scaling of inputs? Derive the scaling required in FFT calculation. **(10 Marks)**

7 a. Design a data memory system with the address range 000800h – 000FFFh for a C5416 processor. Use 2K×8 SRAM memory chips. **(10 Marks)**

   b. What are the features of DMA in C54×× processor? **(04 Marks)**

   c. Explain register sub-addressing technique for configuring DMA. **(06 Marks)**

8 a. With a neat block diagram, explain the synchronous serial interface (SSI) between C54×× and CODEC device. **(10 Marks)**

   b. With a neat block diagram, explain the DSP based biotelemetry receiver system. **(10 Marks)**

* * * * *